REMARKS

Claims 22-30, 33, 70, 74-75, 77-80, and 84-86 have been amended. Claims 1-21, 31-32, 34-69, 72-73, 82-83, and 87-91 have been canceled. Claims 92-100 have been added. Claims 22-30, 33, 70-71, 74-81, 84-86, and 92-100 are now pending. The Title of the Invention has been amended to correspond more closely to the pending claims. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the above-referenced application in light of the amendments and following remarks.

At the outset, Applicants acknowledge with appreciation the indication that dependent claims 30, 32, 77-79, 82-83, and 86 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants respectfully submit, however, that independent claims 22, 70, 75, 80, and 85 have been amended to recite allowable subject matter for at least the reasons provided below.

Claims 24, 26, 29-30, and 85-86 stand rejected under 35 U.S.C. § 112, second paragraph, as having insufficient antecedent basis. The rejection is respectfully traversed. Claims 24, 29-30, and 85 have been amended to maintain proper antecedent basis. Claim 26 depends from amended claim 24 and claim 86 depends from amended claim 85. The § 112, second paragraph, rejection for claims 24, 26, 29-30, and 85-86 should be withdrawn.

Claims 22-24 and 33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,686,331 ("Song"). The rejection is respectfully traversed.

The present invention relates to a gate stack in a transistor structure with at least one channel implant region formed underneath the gate stack. Song does not teach such a structure. Song does not teach a transistor structure comprising, *inter alia*, "a semiconductor substrate; a gate stack with sidewalls . . . comprising: a gate oxide layer . . . a polysilicon layer . . . insulating spacers . . . at least one channel implant region formed underneath said gate stack, wherein said insulating spacers define at least in part the at least one channel implant region; and source and drain regions," as recited in claim 22.

Song merely discloses, in FIG. 2I, LDD region 4, high concentration region 6, dielectric film 10, gate electrode 11, polysilicide 19, first sidewall spacers 13, and second sidewall spacers 14, with substrate 1. Song does not disclose that insulating spacers define at least in part a channel implant region, much less a channel implant region formed underneath the gate stack. Song's first sidewall spacers 13 and second sidewall spacers 14 are not used to define a channel implant region. Song's first sidewall spacers 13 and second sidewall spacers 14 are used to define the location of polysilicide layer 19 (FIG. 2I and 2J).

Accordingly, Song does not disclose each and every element of the claimed structure recited in claim 22. Claims 23-24 and 33 depend from claim 22 and should be similarly allowable along with claim 22 for at least the reasons provided above, and on their own merits. The § 102(b) rejection of claims 22-24 and 33 should be withdrawn.

Claims 22-23 and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,287,925 ("Yu '925"). The rejection is respectfully traversed.

Yu '925 does not teach a transistor structure comprising, *inter alia*, "a semiconductor substrate; a gate stack with sidewalls . . . comprising: a gate oxide layer . . . a polysilicon layer . . . insulating spacers . . . at least one channel implant region formed underneath said gate stack, wherein said insulating spacers define at least in part the at least one channel implant region; and source and drain regions," as recited in claim 22.

Yu '925's FIG. 1 merely illustrates common components of a MOSFET (Col. 1, lines 33-35). In FIG. 1, the transistor consists of a gate oxide 116, polysilicon gate 118, gate silicide 120, spacers 122, and source/drain regions 104, 106. Yu '925 does not teach a channel implant region, much less that insulating spacers define at least in part the channel implant region. Yu '925's spacers 122, in contrast, are used to define source silicide region 114 and drain silicide region 110. As such, Yu '925 does not disclose Applicants' claimed channel implant region formed underneath a gate stack defined at least in part by insulating spacers.

Accordingly, Yu '925 does not disclose each and every element of Applicants' claimed structure recited in claim 22. Claims 23 and 33 depend from claim 22 and should be similarly allowable along with claim 22 for at least the reasons provided above, and on their own merits. The § 102(e) rejection of claims 22-23 and 33 should be withdrawn.

Claims 25-26, 29, 70-71, 74, and 75-76 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Song in view of U.S. Patent No. 6,180,468 ("Yu '468"). The rejection is respectfully traversed.

For similar reasons provided above, Song does not disclose or suggest a transistor structure comprising, *inter alia*, "a semiconductor substrate; a gate stack with

sidewalls . . . comprising: a gate oxide layer . . . a polysilicon layer . . . insulating spacers . . . at least one channel implant region formed underneath said gate stack, wherein said insulating spacers define at least in part the at least one channel implant region; and source and drain regions," as recited in claim 22. Yu '468 is relied upon for disclosing a channel implant region formed underneath a gate stack. Applicants respectfully submit, however, that there is no motivation to combine the cited references since they teach away from each other.

Song relates to "preventing the shorting of the semiconductor device by performing an ion-implantation of an impurity after forming an insulating layer on a gate electrode, and forming sidewall spacers on the upper surface of the gate electrode." (Abstract). Thus, "low and high concentration impurity regions are formed by implanting impurity ions, using an insulating layer as a mask, [such that] the problem that the impurity ions are penetrated through the gate electrode can be solved." (Col. 3, lines 46-50). In other words, Song discloses not to have impurity ions present beneath the gate electrode.

Yu '468, in contrast, discloses forming a channel implant region 38 using nitride spacers 32 and 34 (FIG. 4) underneath gate electrode 50 (FIG. 6). Song explicitly teaches that ion impurities should not be formed underneath the gate electrode. The proposed combination would defeat the very problem that Song is directed to solving: preventing ion impurities from forming underneath the gate electrode. The lack of ion impurities, in Song, avoids a bridging phenomenon between the source and drain (Col. 3, lines 40-45). Accordingly, there is no motivation to combine the references since they teach away from each other. As such, the cited references do not teach or suggest the structure recited in claim 22 since they are not properly combinable.

Similarly, the cited references do not teach or suggest a transistor structure with a gate stack having sidewalls comprising, *inter alia*, "a gate oxide layer . . . a conducting layer . . . sidewall spacers . . . an insulating layer formed adjacent to said sidewall spacers, said insulating layer and sidewall spacers having etched out upper portions that define an area extending beyond a lateral width of said gate stack; and at least one channel implant region formed beneath said gate stack, which is defined at least in part by said area," as recited in claim 70.

As discussed above, Song does not teach or suggest a channel implant region. Further, Song explicitly teaches away from having a channel implant region formed underneath the gate stack. Yu '468 is relied upon for disclosing a channel implant region 38. Yu '468's channel implant region 38, however, is formed self-aligned to gate electrode 50. Thus, the cited references do not teach or suggest the claimed structure, recited in claim 70, since the references are not properly combinable. Moreover, even if the references are combinable, they still would not teach or suggest "an area extending beyond a lateral width of said gate stack; and at least one channel implant region formed beneath said gate stack, which is defined at least in part by said area," as recited in claim 70.

The cited references also do not teach or suggest a transistor structure with a gate stack having sidewalls comprising, *inter alia*, "a gate oxide layer . . . a conducting layer . . . first sidewall spacers provided adjacent to the sidewalls of said gate stack; second sidewall spacers provided over said conducting layer; and at least one channel implant region formed underneath said gate stack . . . wherein said at least one channel implant region is narrower in width than said gate stack," as recited in claim 75.

As discussed above, there is no motivation to combine the references since they teach away from each other. Further, Yu '468's channel implant region 38 is formed self-aligned to gate electrode 50. Yu '468's channel implant region 38 is not narrower than the gate stack. Thus, even if the references are properly combinable, they still would not disclose or suggest "at least one channel implant region [which] is narrower in width than said gate stack," as recited in claim 75.

Moreover, Song and Yu '468, even in combination, do not disclose or suggest "second sidewall spacers provided over said conducting layer," as recited in claim 75. Yu '468's FIG. 4 discloses that nitride spacers 32 and 34, which arguably correspond to Applicants' claimed second sidewall spacers, are formed on gate oxide layer 22 and not on conducting layer 50 (FIG. 6). Song does not even teach or suggest the presence of second sidewall spacers.

Claims 25-26 and 29 depend from claim 22 and should be similarly allowable along with claim 22 for at least the reasons provided above, and on their own merits. Moreover, the cited references do not teach or suggest a channel implant region that "is narrower than the width of said gate stack," as recited in dependent claim 26, or that "second insulating spacers are provided over said polysilicon layer," as recited in dependent claim 29. These are additional reasons for the allowance of claims 25 and 26.

Claims 71 and 74 depend from claim 70 and should be similarly allowable along with claim 70 for at least the reasons provided above, and on their own merits. Claim 76 depends from claim 75 and should be similarly allowable along with claim 75 for at least the reasons provided above, and on its own merits.

Claims 25, 70-71, and 74 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu '925 in view of Yu '468. The rejection is respectfully traversed.

For similar reasons provided above, claims 25, 70-71, and 74 should be allowable over the cited references. For example, Yu '925 does not teach or suggest a channel implant region formed underneath a gate stack. Yu '468 is relied upon for disclosing a channel implant region formed underneath a gate stack. The cited references however, even in combination, still would not teach or suggest a transistor structure with a gate stack having sidewalls comprising, *inter alia*, "a gate oxide layer . . . a conducting layer . . . sidewall spacers . . . an insulating layer formed adjacent to said sidewall spacers, said insulating layer and sidewall spacers having etched out upper portions that define an area extending beyond a lateral width of said gate stack; and at least one channel implant region formed beneath said gate stack, which is defined at least in part by said area," as recited in claim 70. As discussed previously, Yu '468's channel implant region 38 is formed self-aligned to gate electrode 50. Combining the references still would not yield "an area extending beyond a lateral width of said gate stack; and at least one channel implant region formed beneath said gate stack, which is defined at least in part by said area," as recited in claim 70.

Moreover, there is no motivation to combine the cited references to teach or suggest the subject matter of claims 25, 70-71, and 74. Yu '925 discloses a spacer liner oxide 218 used as a buffer layer between spacer 216 and the sidewalls of gate structure 204, gate oxide 202, and gate capping layer 206 (Col. 5, lines 19-26). Yu '925's gate structure employs preamorphization crystallized regions 208, 210, 220, and 222. These regions are highly doped with dopants that are recrystallized to achieve abrupt junctions with low series resistance (Col. 7, lines 9-32).

There is no motivation to use Yu '468's nitride spacers 32 and 34 to form a channel implant region 38 underneath Yu '925's gate electrode 204. Employing Yu '468's nitride spacers 32 and 34 would prevent Yu '925's regions 208 and 210 from receiving dopants (FIG. 7). These dopants are used to recrystallize regions 208 and 210 to form regions 242 and 244 by a laser thermal anneal process. The proposed combination would defeat the very problem that Yu '925 is directed to solving: reducing resistances by preamorphization crystallized regions, since Yu '468's nitride spacers 32 and 34 would prevent the dopants from entering regions 208 and 210. Accordingly, the proposed combination does not teach or disclose the subject matter recited in claims 25, 70-71, and 74 since there is no motivation to combine the references. Claim 25 depends from claim 22 and should be allowable over the prior art of record with claim 22, and on its own merits.

Claims 27, 28, 31, 72-73, 80-81, and 84 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu '925, in view of Yu '468, and further in view of U.S. Patent No. 6,043,545 ("Tseng"). The rejection is respectfully traversed.

For similar reasons provided above, there is no motivation to combine Yu '925 and Yu '468. The proposed combination defeats the very problem that Yu '925 is directed to solving: reducing resistances by creating preamorphization crystallized regions. Employing Yu '468's nitride spacers 32 and 34 would prevent Yu '925's regions 208 and 210 from receiving dopants that recrystallize (FIG. 7). For at least this reason, claims 27, 28, 31, 72-73, 80-81, and 84 should be allowable over Yu '925 and Yu '468, since there is no motivation to combine the references.

Tseng is relied upon for disclosing an insulating layer with sidewall spacer top portions that have been etched, and adds nothing to rectify the deficiencies associated with Yu '925 and Yu '468. Moreover, there is no motivation to combine

Tseng with Yu '468 and Yu '925. As described above, Yu '468 and Yu '925 are not properly combinable. Still further, Yu '468 discloses a channel implant region 38 that is self-aligned to the gate electrode 50. Combining Tseng with Yu '468 would result in a channel implant region 38 that is not self-aligned. Accordingly, there is no motivation to combine any of the cited references since they teach away from the proposed combination.

Claims 27 and 28 depend from claim 22 and should be similarly allowable along with claim 22 for at least the reasons provided above, and on their own merits. Moreover, even in combination, the cited references still would not teach or suggest the subject matter recited in claims 27 and 28. The cited references do not teach or suggest "an insulating layer adjacent to said sidewall spacers, said insulating layer and said sidewall spacers having at least a portion of their upper surfaces removed to define an area extending beyond a lateral width of said gate stack," as recited in claim 27. Claim 28 depends from claim 27 and recites that the "at least one channel implant region is defined at least in part by said area." As discussed previously, Yu '468's channel implant region 38 is formed self-aligned to gate electrode 50 and is not wider than the gate stack. These are additional reasons for the allowance of dependent claims 27 and 28.

Similarly, the cited references do not teach or suggest a transistor structure with a gate stack having sidewall spacers comprising, *inter alia*, "a gate oxide layer . . . a conducting layer . . . first sidewall spacers provided adjacent to the sidewalls of said gate stack; an insulating layer formed adjacent to said first sidewall spacers . . . having etched out portions that define an area extending beyond a lateral width of said gate stack; a first channel implant region . . . and a second channel implant region formed within said first channel implant region," as recited in claim 80.

The cited references do not disclose or suggest "a second channel implant region formed within said first channel implant region," as recited in claim 80. Moreover, the cited references do not teach or suggest a first channel implant region that extends beyond a lateral width of the gate stack. Yu '468's channel implant region 38 is formed self-aligned to gate electrode 50. Claims 81 and 84 depend from claim 80 and should be similarly allowable with claim 80, and on their own merits.

Moreover, the prior art of record does not teach or suggest the subject matter of newly added claims 92-100. The prior art of record does not teach or suggest a gate stack with sidewalls comprising "an oxide layer . . . a conducting layer . . . a first set of spacers provided on each side of said gate stack with a second set of spacers provided over said conducting layer; and a first channel implant region formed underneath said gate stack . . . wherein the first set of spacers or second set of spacers define at least in part the width of said channel implant region," as recited in claim 92.

The prior art of record does not teach or suggest "a second channel implant region formed within the first channel implant region, wherein said second channel implant region is narrower in width than said first channel implant region," as recited in claim 95. The cited references simply do not teach or suggest a second channel implant region formed within the first channel implant region, much less one that is narrower in width than the first channel implant region. Similarly, the prior art of record does not teach or suggest "a second channel implant region formed within said first channel implant region," as recited in claim 100.

The prior art of record does not teach or suggest a "first channel implant region [which] is narrower in width than said gate stack," as recited in claim 97. As discussed previously, in the most favorable light, the prior art of record merely discloses a channel implant region that is self-aligned to a gate stack. As such, the prior

art of record would also not teach or suggest a "first channel implant region [which] is wider than said gate stack," as recited in claim 99.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: January 28, 2005

Respectfully submitted,

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